

REMARKS

Reconsideration of the present application is respectfully requested. Claim 1 has been amended. Claim 2 has been canceled. Claims 3-68 have been newly added. No new matter has been added.

Claim Rejections

Claim 1 stands rejected under 35 USC §102(e) based on Kever (US Pat. No. 6,735,673). Applicant respectfully traverses the rejections.

The present application discloses a mechanism of compressing two or more cache lines' worth of information into one compressed cache line's worth of information. The compressed cache line's worth of information is then stored back into a program-addressable memory, the system memory of a computing system, for example (as opposed to cache memory that is much faster than the system memory). Thus, rather than requiring two or more system memory accesses to fetch the two or more cache lines' worth of information from, one system memory access is able to fetch the compressed cache line's worth of information and then decompress it into the original two or more cache lines' worth of information. This advantageously reduces the demand for system memory accesses so as to make the system memory's usage more efficient within the computing system.

Claim 1 recites:

1. A memory controller for use in **a system having a program-addressable memory controlled by the memory controller and a processor coupled with the memory by an external bus**, the memory controller comprising a

compression map cache to store information that identifies a **compressed cache line's worth of information stored in the memory**, the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information.
(emphasis added).

By contrast, Kever does not teach or suggest the above emphasized limitations.

Kever discloses a mechanism of storing compressed data in a cache so that more data may be cached in order to increase the probability of a cache hit (*see* Kever's abstract). The compressed lines of data is stored in a cache, rather than in a program-addressable memory, such as recited in claim 1.

Because Kever does not teach or suggest the all limitations of claim 1, claim 1 is not anticipated by Kever.


Similarly, the newly added independent claims 17, 33, 44 and 57 each recites similar limitations as discussed above for claim 1. For similar reasons, claims 17, 33, 44, 57 and all claims which depend on them are also patentable over Kever.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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